FIG.1

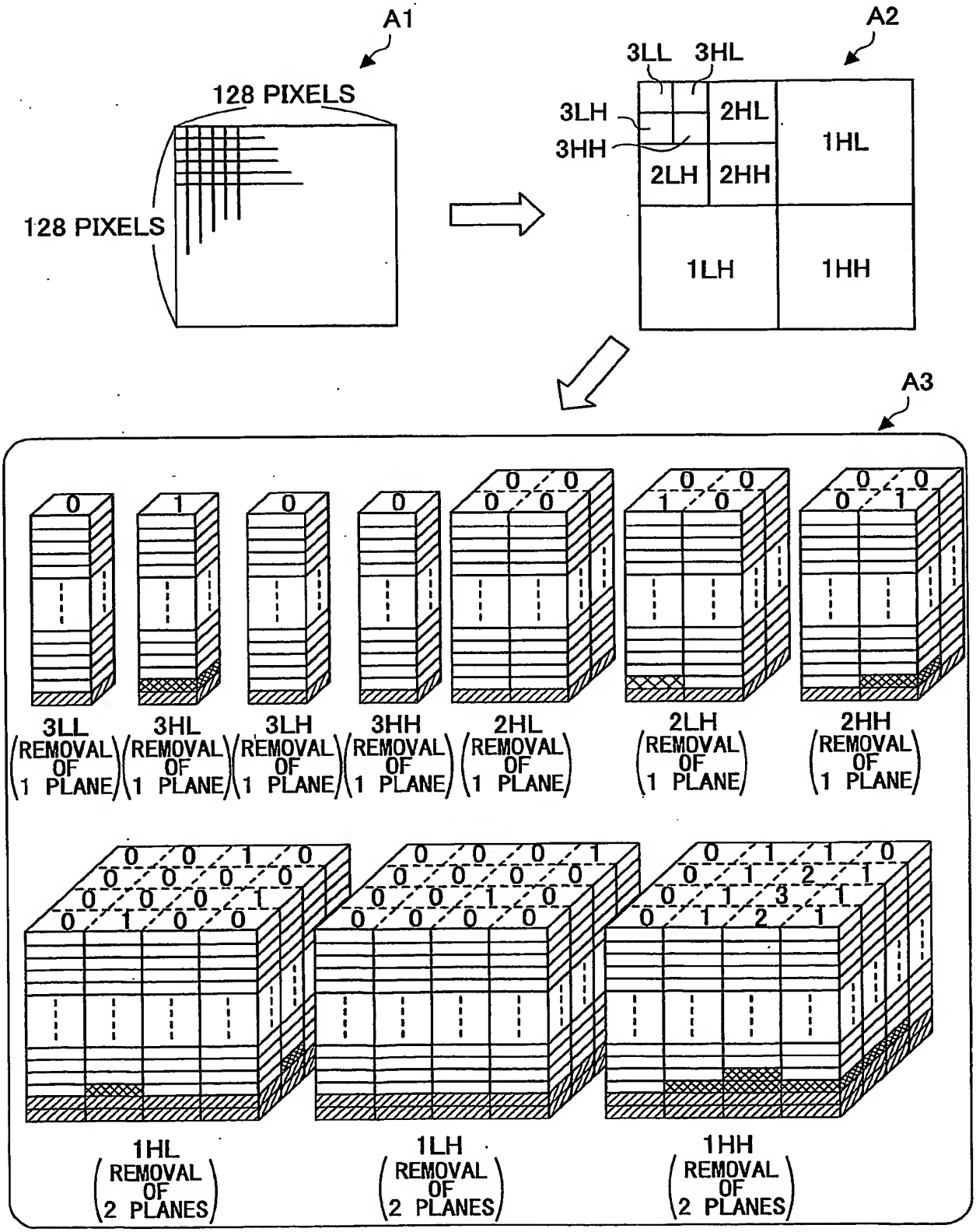

A1
128 PIXELS
128 PIXELS
A2
3LL
3HL
3LH
3HH
2HL
1HL
2LH
2HH
1LH
1HH
A3
3LL (REMOVAL OF 1 PLANE)
3HL (REMOVAL OF 1 PLANE)
3LH (REMOVAL OF 1 PLANE)
3HH (REMOVAL OF 1 PLANE)
2HL (REMOVAL OF 1 PLANE)
2LH (REMOVAL OF 1 PLANE)
2HH (REMOVAL OF 1 PLANE)
1HL (REMOVAL OF 2 PLANES)
1LH (REMOVAL OF 2 PLANES)
1HH (REMOVAL OF 2 PLANES)

FIG.2

DATA No. T	Y 3LL, 3HL-LH-HH, 2HL-LH-HH, 1HL-LH-HH Cb 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH Cr 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH	DATA No. T	Y 3LL, 3HL-LH-HH, 2HL-LH-HH, 1HL-LH-HH Cb 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH Cr 3LL, 3HL-LH-HH 2HL-LH-HH, 1HL-LH-HH
T=0	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 1 0, 0 0 0, 0 0 0, 0 0 0	T=399	1, 1 1 3, 4 4 6, 101017 9, 101013, 141418, 202027 8, 9 911, 121216, 181823
T=1	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 2 0, 0 0 0, 0 0 0, 0 0 0	T=400	1, 1 1 3, 4 4 6, 101017 9, 101013, 141418, 202027 8, 9 911, 121216, 181823
T=2	0, 0 0 0, 0 0 0, 0 0 0 0, 0 0 0, 0 0 0, 0 0 3 0, 0 0 0, 0 0 0, 0 0 0	⋮	⋮
⋮	⋮	T=499	
T=99	0, 0 0 0, 0 0 0, 0 0 6 0, 0 0 3, 4 4 8, 101017 0, 0 0 1, 2 2 6, 7 713	T=500	
T=100	0, 0 0 0, 0 0 0, 0 0 7 0, 0 0 3, 4 4 8, 101017 0, 0 0 1, 2 2 6, 7 713	⋮	⋮
⋮	⋮	T=1000	
T=199	0, 0 0 0, 0 0 0, 5 511 3, 4 4 7, 8 813, 151521 2, 3 3 6, 7 710, 121217	⋮	⋮
T=200	0, 0 0 0, 0 0 0, 5 511 3, 4 4 7, 8 813, 151522 2, 3 3 6, 7 710, 121217	T=1500	
⋮	⋮	⋮	⋮
T=299	0, 0 0 0, 1 1 4, 8 814 6, 7 710, 111216, 181825 6, 6 6 9, 101013, 151520	⋮	⋮
T=300	0, 0 0 0, 1 1 4, 8 814 6, 7 710, 121216, 181825 6, 6 6 9, 101013, 151520	⋮	⋮
⋮	⋮	⋮	⋮

FIG.3

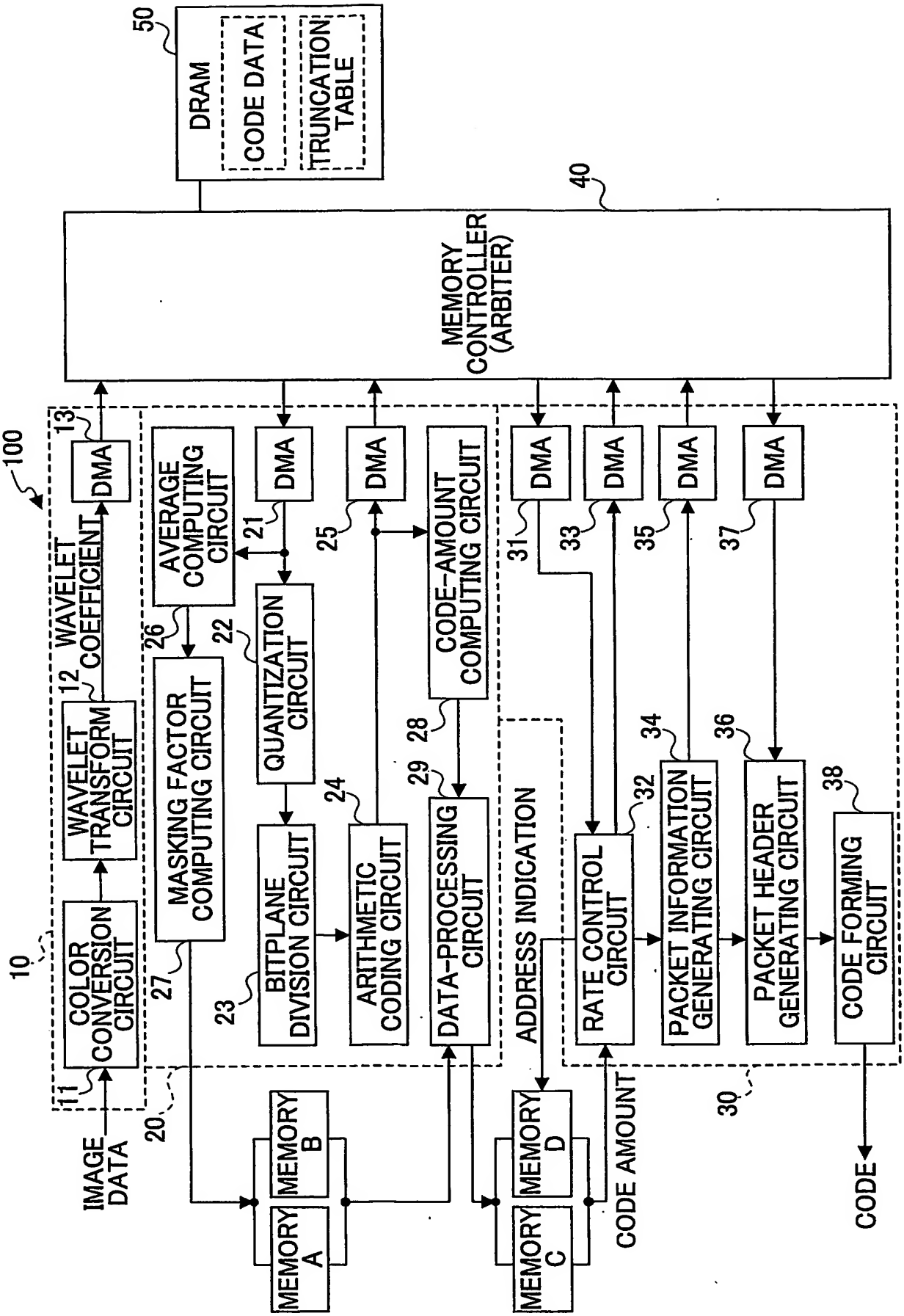

50
DRAM
CODE DATA
TRUNCATION TABLE
40
MEMORY CONTROLLER (ARBITER)
100
10
11
IMAGE DATA
COLOR CONVERSION CIRCUIT
12
WAVELET TRANSFORM CIRCUIT
WAVELET COEFFICIENT
13
DMA
20
MASKING FACTOR COMPUTING CIRCUIT
27
AVERAGE COMPUTING CIRCUIT
26
21
DMA
22
QUANTIZATION CIRCUIT
23
BITPLANE DIVISION CIRCUIT
24
ARITHMETIC CODING CIRCUIT
25
DMA
28
CODE-AMOUNT COMPUTING CIRCUIT
29
DATA-PROCESSING CIRCUIT
MEMORY A
MEMORY B
MEMORY C
MEMORY D
ADDRESS INDICATION
CODE AMOUNT
31
DMA
33
DMA
32
RATE CONTROL CIRCUIT
34
PACKET INFORMATION GENERATING CIRCUIT
35
DMA
36
PACKET HEADER GENERATING CIRCUIT
37
DMA
38
CODE FORMING CIRCUIT
30
CODE

FIG.4

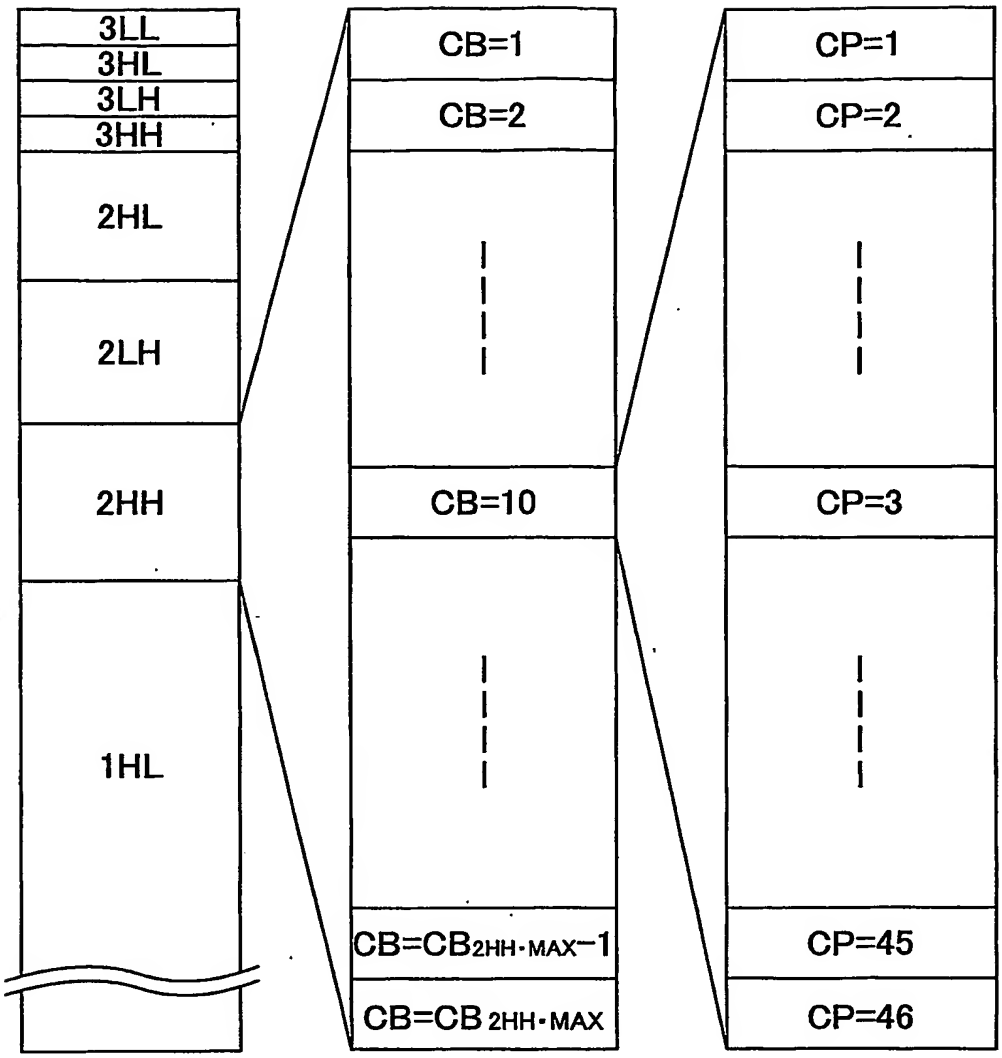

3LL
3HL
3LH
3HH
2HL
2LH
2HH
1HL
CB=1
CB=2
CB=10
CB=CB2HH·MAX−1
CB=CB2HH·MAX
CP=1
CP=2
CP=3
CP=45
CP=46

FIG.5

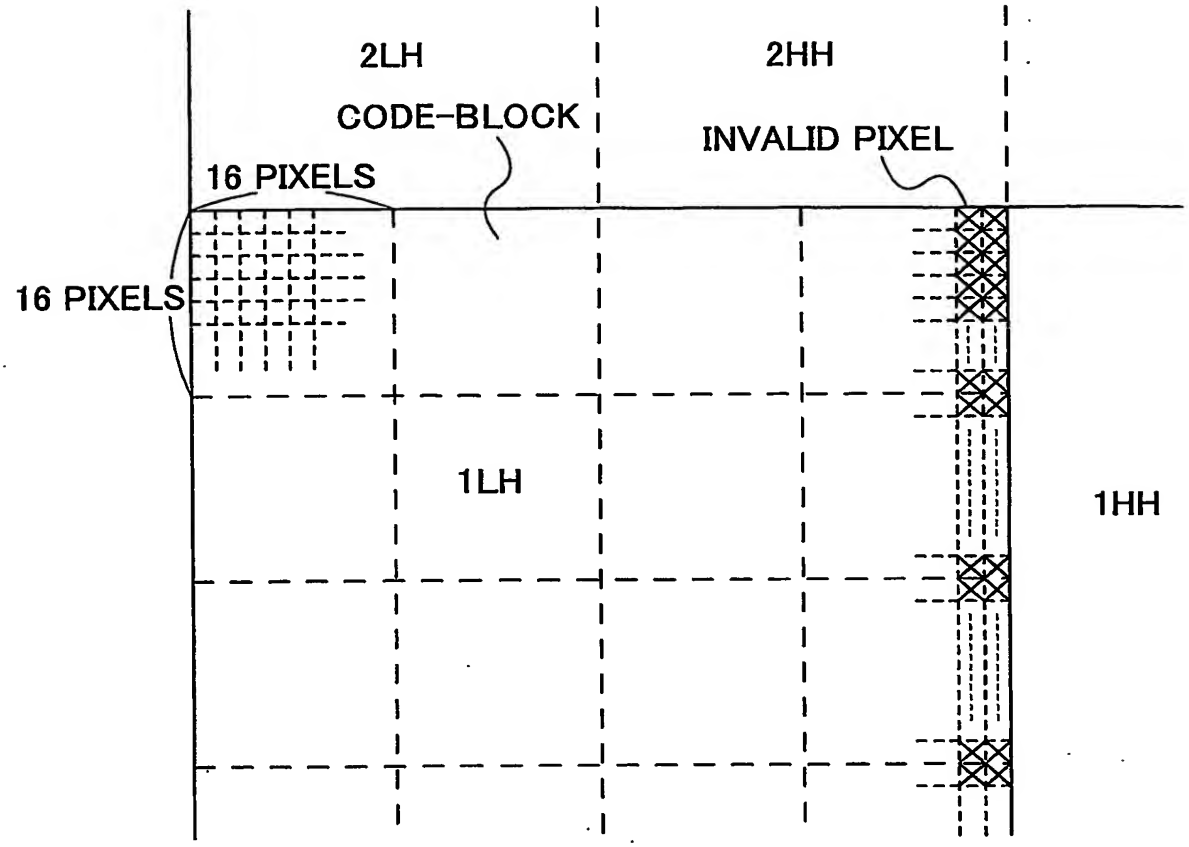


FIG.6

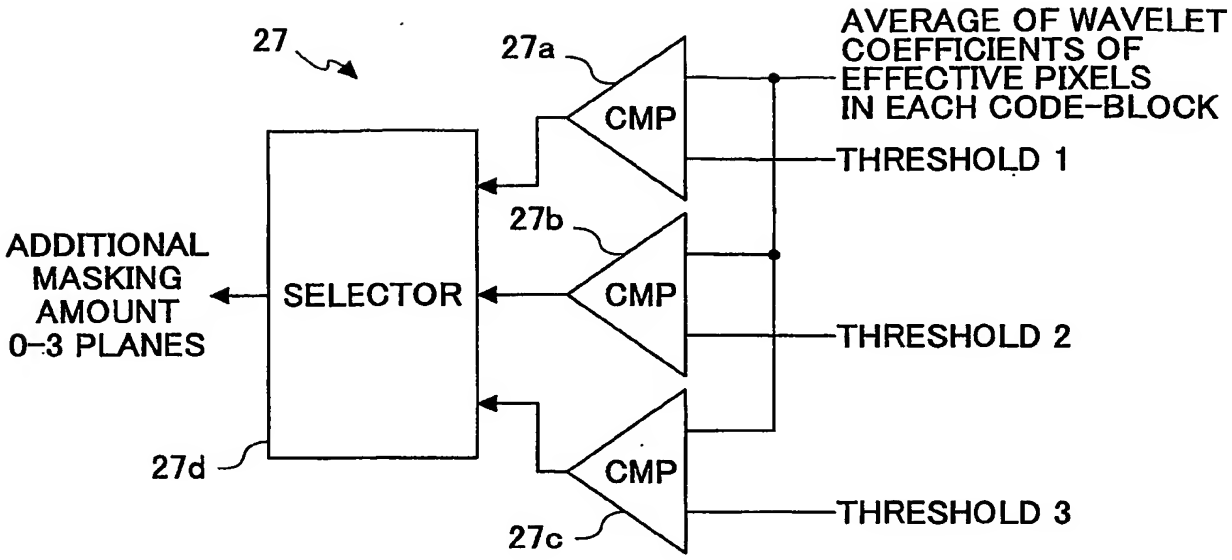

27
27a
CMP
AVERAGE OF WAVELET COEFFICIENTS OF EFFECTIVE PIXELS IN EACH CODE-BLOCK
THRESHOLD 1
27b
CMP
THRESHOLD 2
ADDITIONAL MASKING AMOUNT 0-3 PLANES
SELECTOR
27d
CMP
THRESHOLD 3
27c

FIG.7

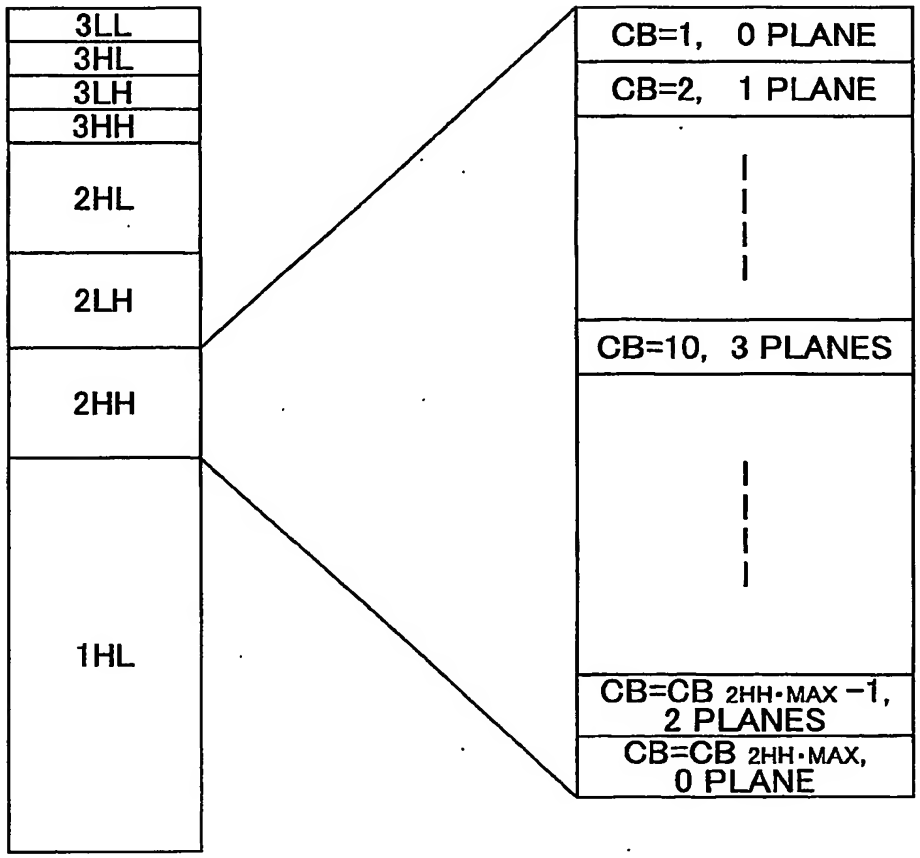

3LL
3HL
3LH
3HH
2HL
2LH
2HH
1HL
CB=1, 0 PLANE
CB=2, 1 PLANE
CB=10, 3 PLANES
CB=CB 2HH·MAX −1, 2 PLANES
CB=CB 2HH·MAX, 0 PLANE

FIG.8

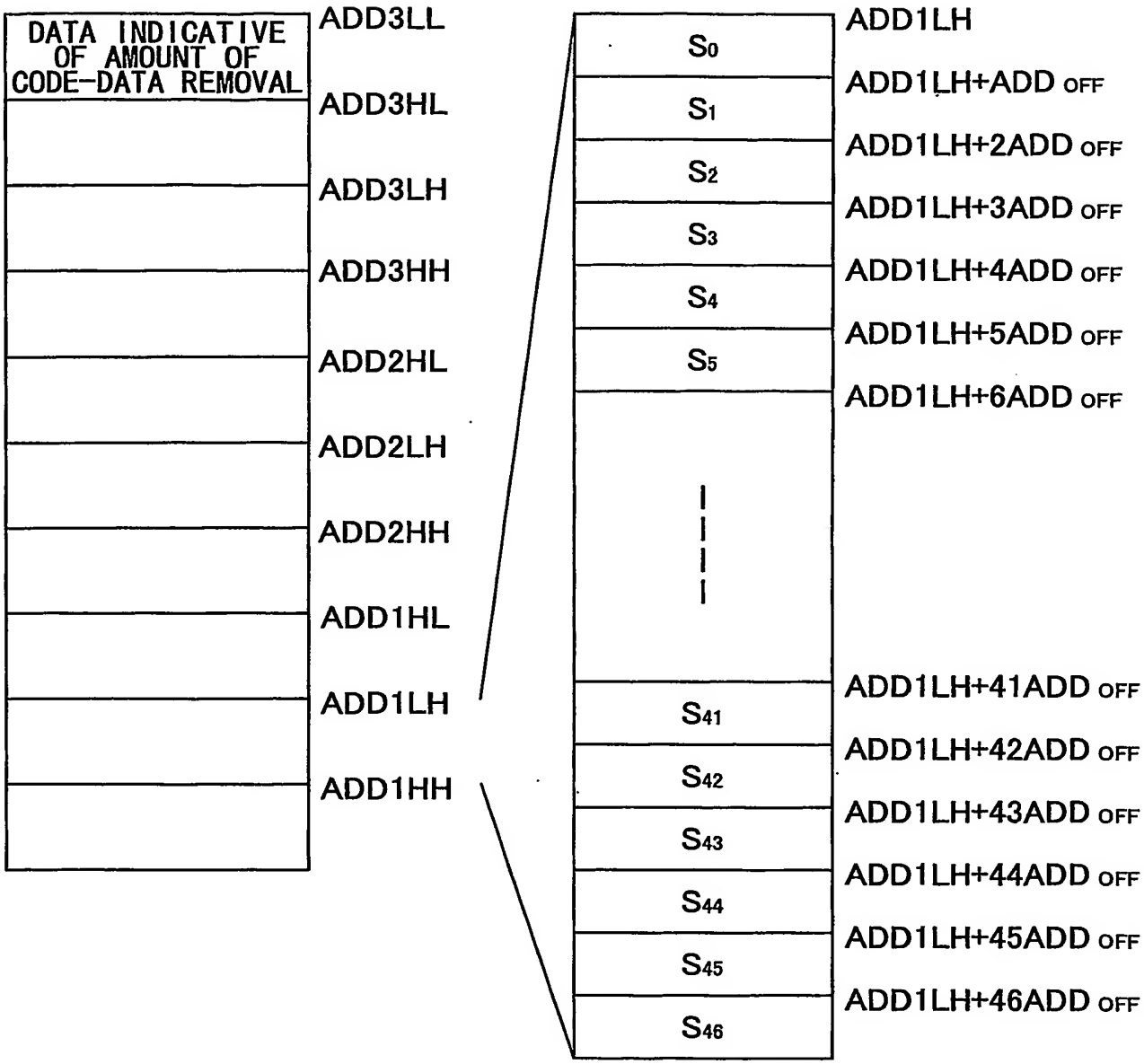

DATA INDICATIVE OF AMOUNT OF CODE-DATA REMOVAL
ADD3LL
ADD3HL
ADD3LH
ADD3HH
ADD2HL
ADD2LH
ADD2HH
ADD1HL
ADD1LH
ADD1HH
S0
S1
S2
S3
S4
S5
S41
S42
S43
S44
S45
S46
ADD1LH
ADD1LH+ADD OFF
ADD1LH+2ADD OFF
ADD1LH+3ADD OFF
ADD1LH+4ADD OFF
ADD1LH+5ADD OFF
ADD1LH+6ADD OFF
ADD1LH+41ADD OFF
ADD1LH+42ADD OFF
ADD1LH+43ADD OFF
ADD1LH+44ADD OFF
ADD1LH+45ADD OFF
ADD1LH+46ADD OFF

FIG.9

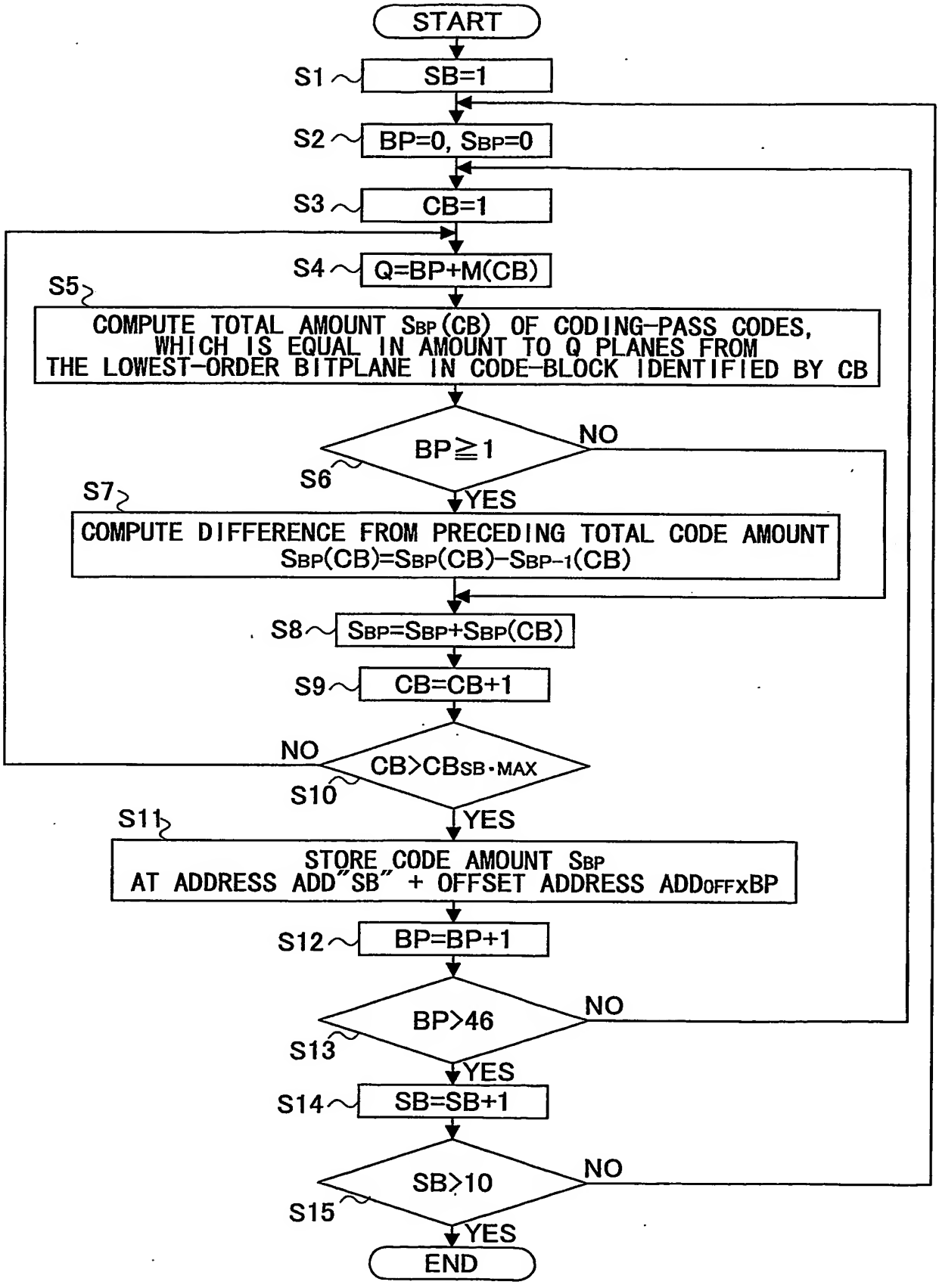

START
S1
SB=1
S2
BP=0, SBP=0
S3
CB=1
S4
Q=BP+M(CB)
S5
COMPUTE TOTAL AMOUNT SBP(CB) OF CODING-PASS CODES, WHICH IS EQUAL IN AMOUNT TO Q PLANES FROM THE LOWEST-ORDER BITPLANE IN CODE-BLOCK IDENTIFIED BY CB
S6
BP≧1
NO
YES
S7
COMPUTE DIFFERENCE FROM PRECEDING TOTAL CODE AMOUNT
SBP(CB)=SBP(CB)-SBP-1(CB)
S8
SBP=SBP+SBP(CB)
S9
CB=CB+1
S10
CB>CBSB·MAX
NO
YES
S11
STORE CODE AMOUNT SBP AT ADDRESS ADD"SB" + OFFSET ADDRESS ADDOFFXBP
S12
BP=BP+1
S13
BP>46
NO
YES
S14
SB=SB+1
S15
SB>10
NO
YES
END

FIG.10

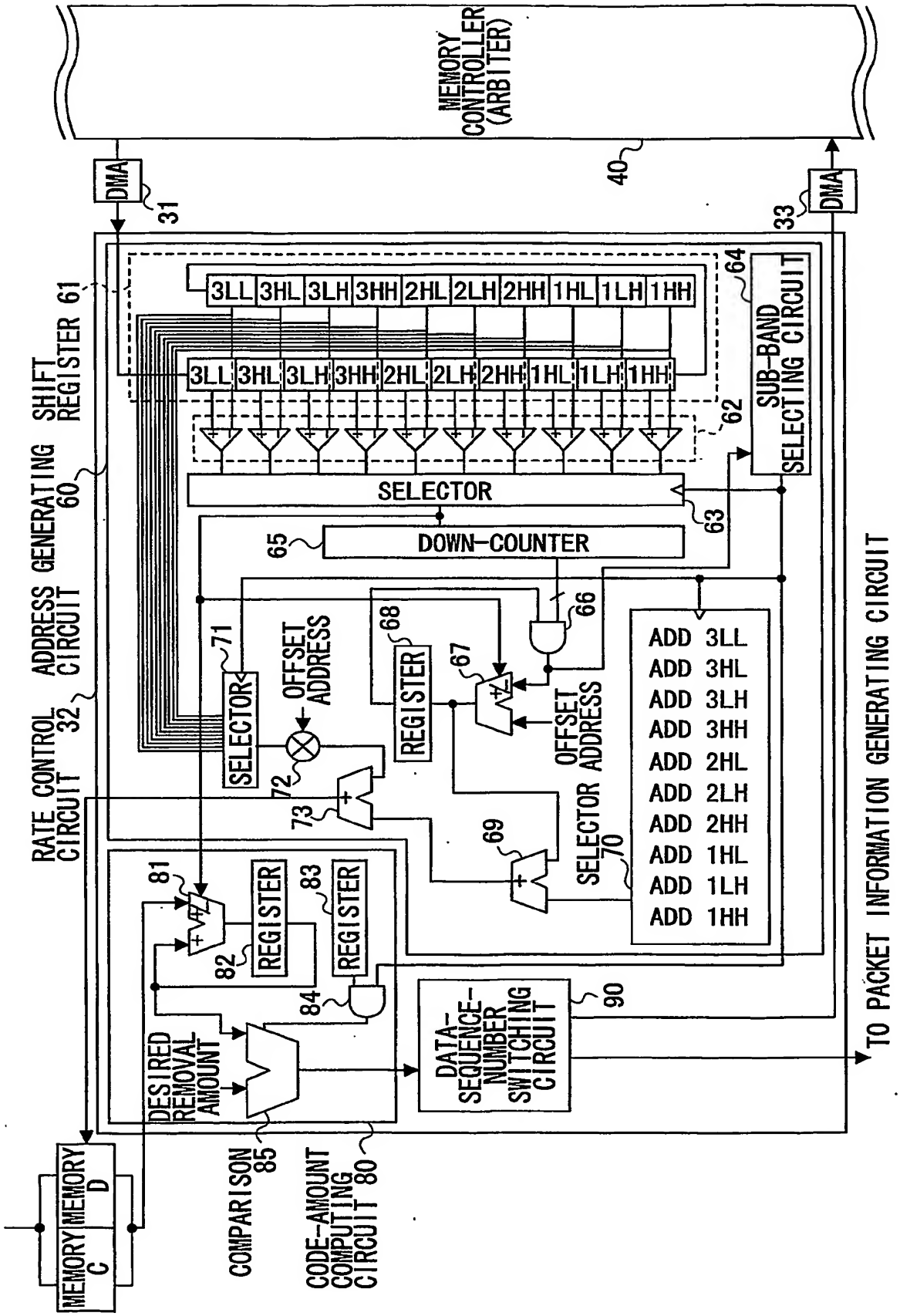

MEMORY CONTROLLER (ARBITER)
40
DMA
31
DMA
33
SHIFT REGISTER 61
3LL 3HL 3LH 3HH 2HL 2LH 2HH 1HL 1LH 1HH
SUB-BAND SELECTING CIRCUIT
64
62
SELECTOR
63
DOWN-COUNTER
65
ADDRESS GENERATING CIRCUIT 60
RATE CONTROL CIRCUIT 32
SELECTOR
71
OFFSET ADDRESS
72
REGISTER
68
67
66
OFFSET ADDRESS
73
69
SELECTOR
70
ADD 3LL
ADD 3HL
ADD 3LH
ADD 3HH
ADD 2HL
ADD 2LH
ADD 2HH
ADD 1HL
ADD 1LH
ADD 1HH
81
82
REGISTER
83
REGISTER
84
DESIRED REMOVAL AMOUNT
DATA-SEQUENCE-NUMBER SWITCHING CIRCUIT
90
TO PACKET INFORMATION GENERATING CIRCUIT
MEMORY C
MEMORY D
COMPARISON 85
CODE-AMOUNT COMPUTING CIRCUIT 80

FIG.11

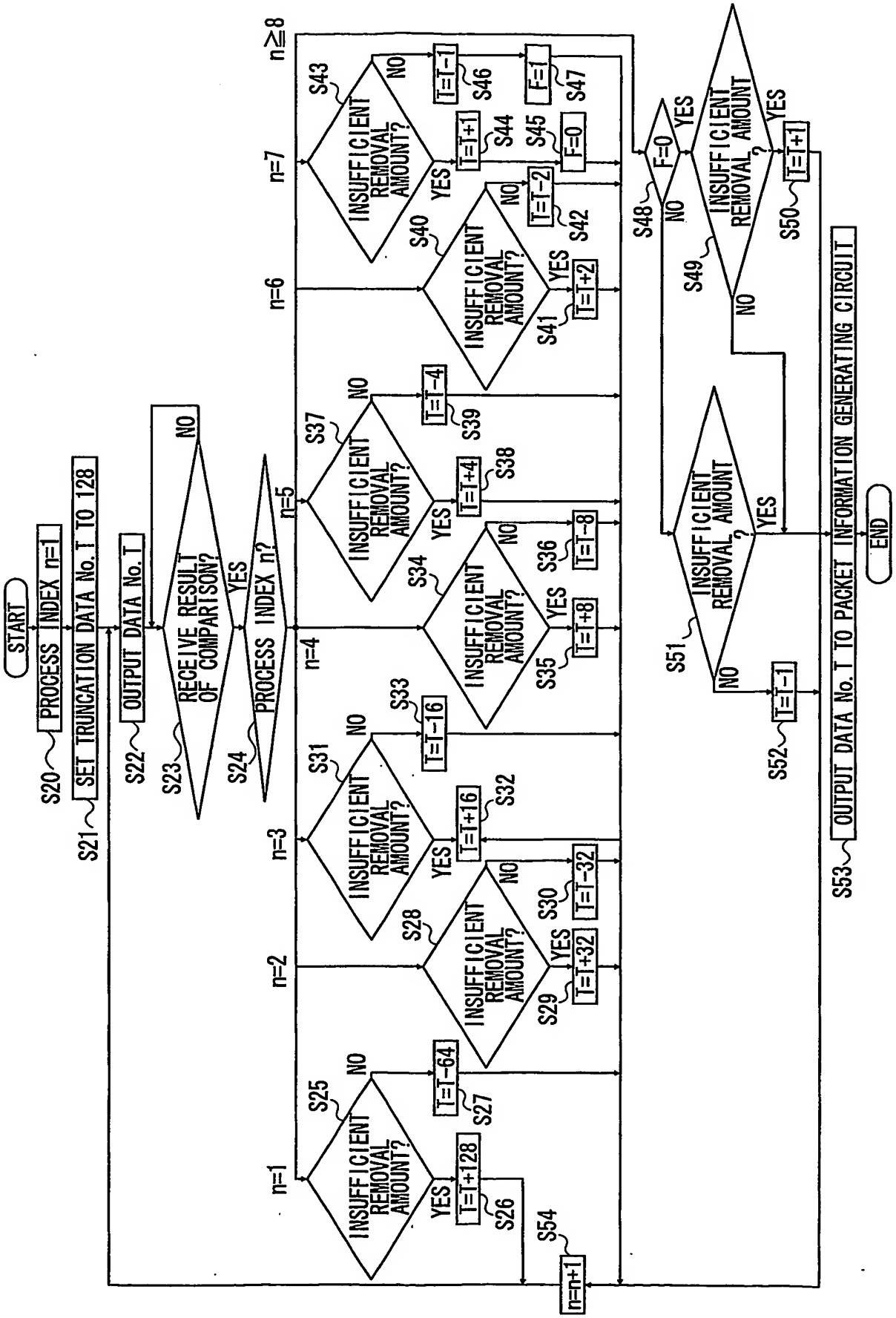

START
S20
PROCESS INDEX n=1
S21
SET TRUNCATION DATA No. T TO 128
S22
OUTPUT DATA No. T
S23
RECEIVE RESULT OF COMPARISON?
NO
YES
S24
PROCESS INDEX n?
n=1
n=2
n=3
n=4
n=5
n=6
n=7
n≧8
S25
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T-64
S27
T=T+128
S26
S28
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T-32
S30
T=T+32
S29
S31
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T-16
S33
T=T+16
S32
S34
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T-8
S36
T=T+8
S35
S37
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T-4
S39
T=T+4
S38
S40
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T-2
S42
T=T+2
S41
S43
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T-1
S46
F=1
S47
T=T+1
S44
F=0
S45
S48
F=0
NO
YES
S49
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T+1
S50
S51
INSUFFICIENT REMOVAL AMOUNT?
NO
YES
T=T-1
S52
S53
OUTPUT DATA No. T TO PACKET INFORMATION GENERATING CIRCUIT
END
S54
n=n+1

FIG.12

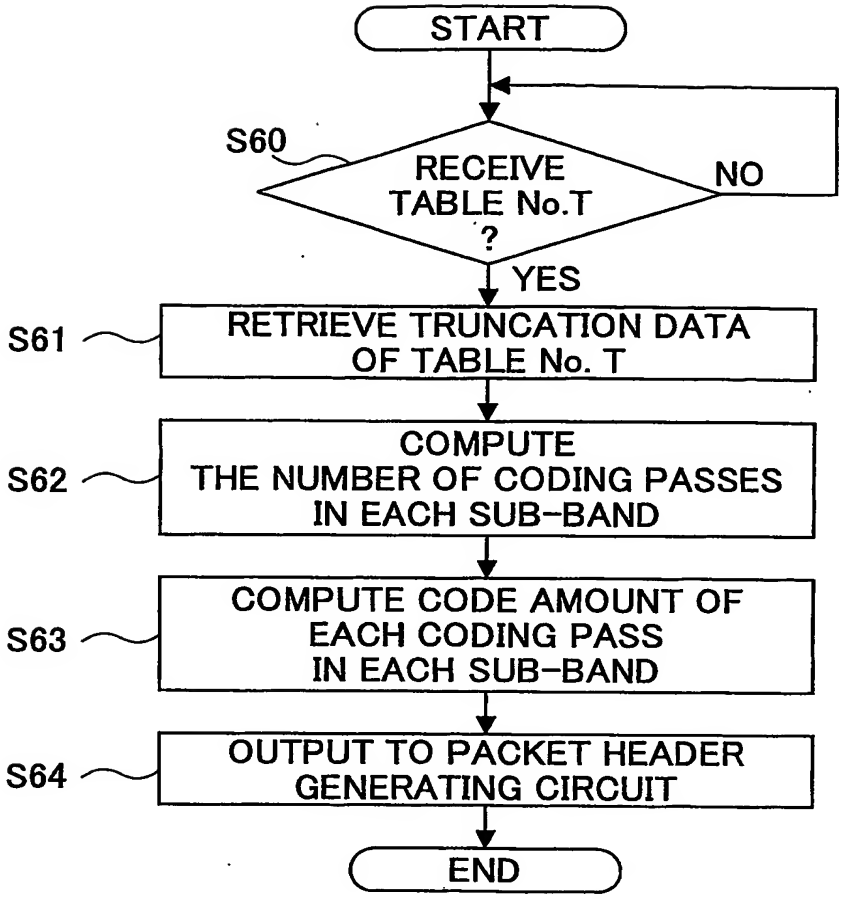

START
S60
RECEIVE TABLE No.T ?
NO
YES
S61
RETRIEVE TRUNCATION DATA OF TABLE No. T
S62
COMPUTE THE NUMBER OF CODING PASSES IN EACH SUB-BAND
S63
COMPUTE CODE AMOUNT OF EACH CODING PASS IN EACH SUB-BAND
S64
OUTPUT TO PACKET HEADER GENERATING CIRCUIT
END

FIG.13

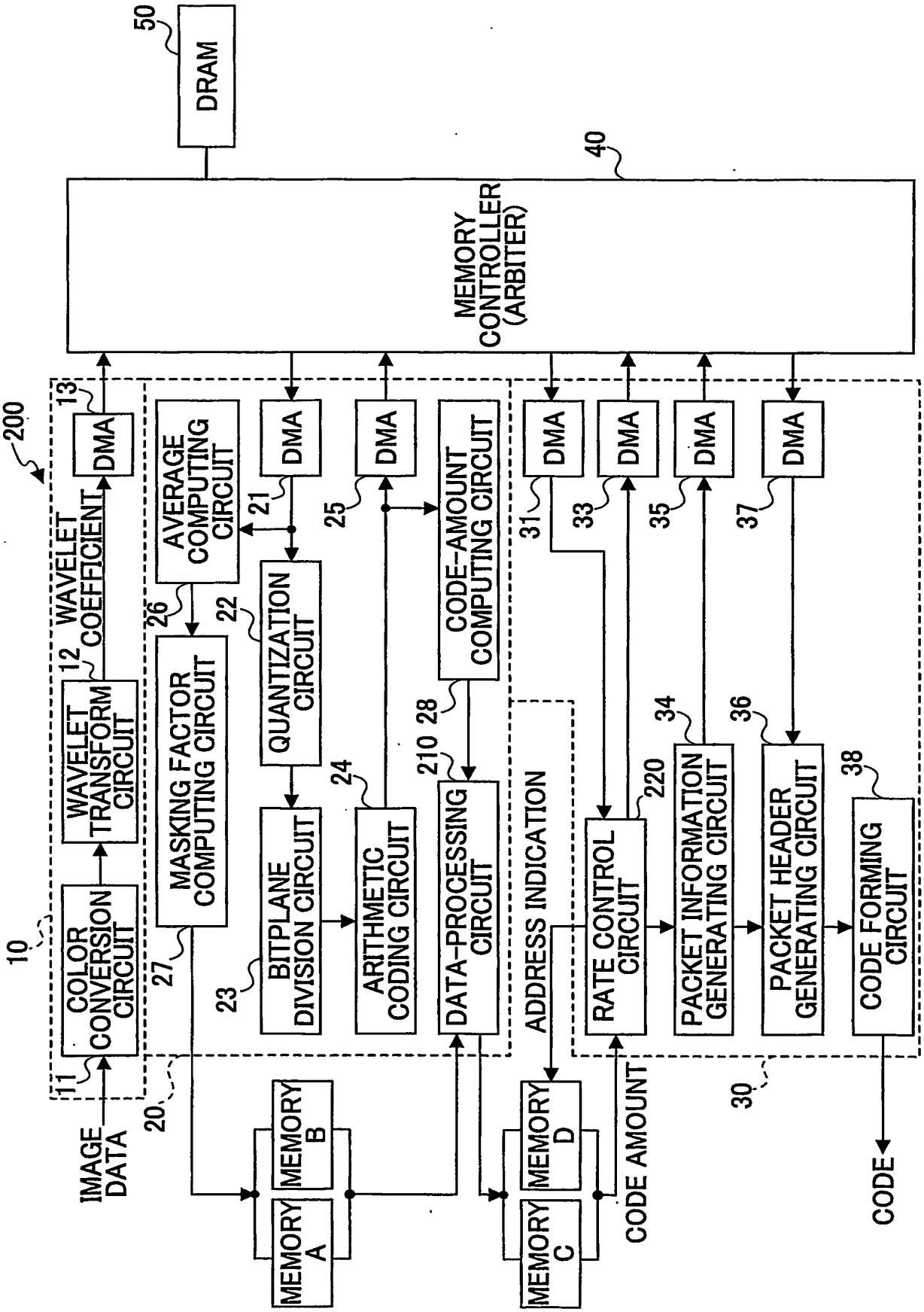

50
DRAM
40
MEMORY CONTROLLER (ARBITER)
200
10
11
COLOR CONVERSION CIRCUIT
12
WAVELET TRANSFORM CIRCUIT
WAVELET COEFFICIENT
13
DMA
20
IMAGE DATA
MEMORY A
MEMORY B
MEMORY C
MEMORY D
27
MASKING FACTOR COMPUTING CIRCUIT
26
AVERAGE COMPUTING CIRCUIT
21
DMA
22
QUANTIZATION CIRCUIT
23
BITPLANE DIVISION CIRCUIT
24
ARITHMETIC CODING CIRCUIT
25
DMA
28
CODE-AMOUNT COMPUTING CIRCUIT
210
DATA-PROCESSING CIRCUIT
ADDRESS INDICATION
31
DMA
33
DMA
220
RATE CONTROL CIRCUIT
CODE AMOUNT
35
DMA
34
PACKET INFORMATION GENERATING CIRCUIT
37
DMA
36
PACKET HEADER GENERATING CIRCUIT
38
CODE FORMING CIRCUIT
30
CODE

FIG.14

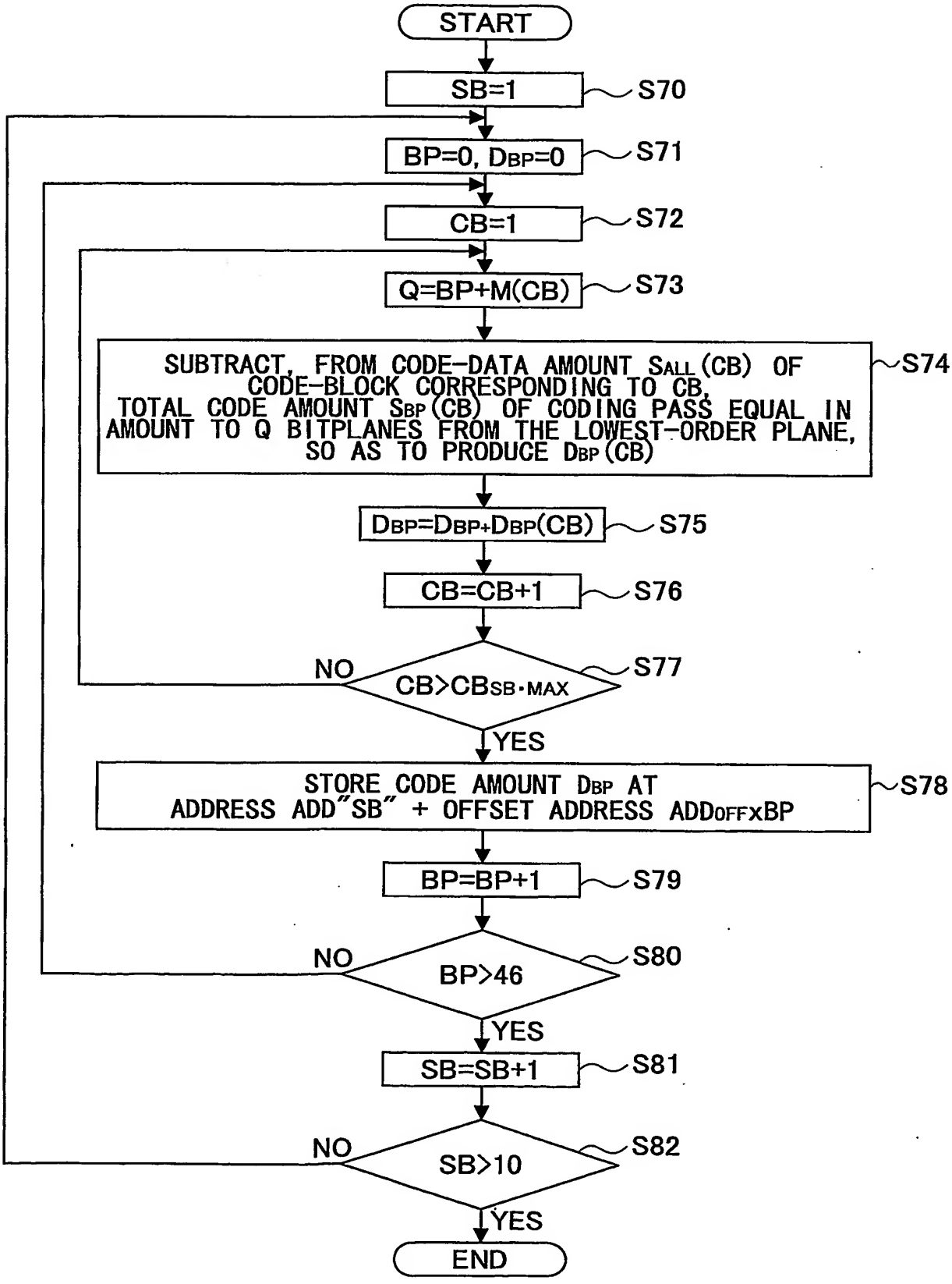

START
SB=1
S70
BP=0, DBP=0
S71
CB=1
S72
Q=BP+M(CB)
S73
SUBTRACT, FROM CODE-DATA AMOUNT SALL(CB) OF CODE-BLOCK CORRESPONDING TO CB, TOTAL CODE AMOUNT SBP(CB) OF CODING PASS EQUAL IN AMOUNT TO Q BITPLANES FROM THE LOWEST-ORDER PLANE, SO AS TO PRODUCE DBP(CB)
S74
DBP=DBP+DBP(CB)
S75
CB=CB+1
S76
NO
CB>CBSB·MAX
S77
YES
STORE CODE AMOUNT DBP AT ADDRESS ADD"SB" + OFFSET ADDRESS ADDOFFxBP
S78
BP=BP+1
S79
NO
BP>46
S80
YES
SB=SB+1
S81
NO
SB>10
S82
YES
END

FIG.15

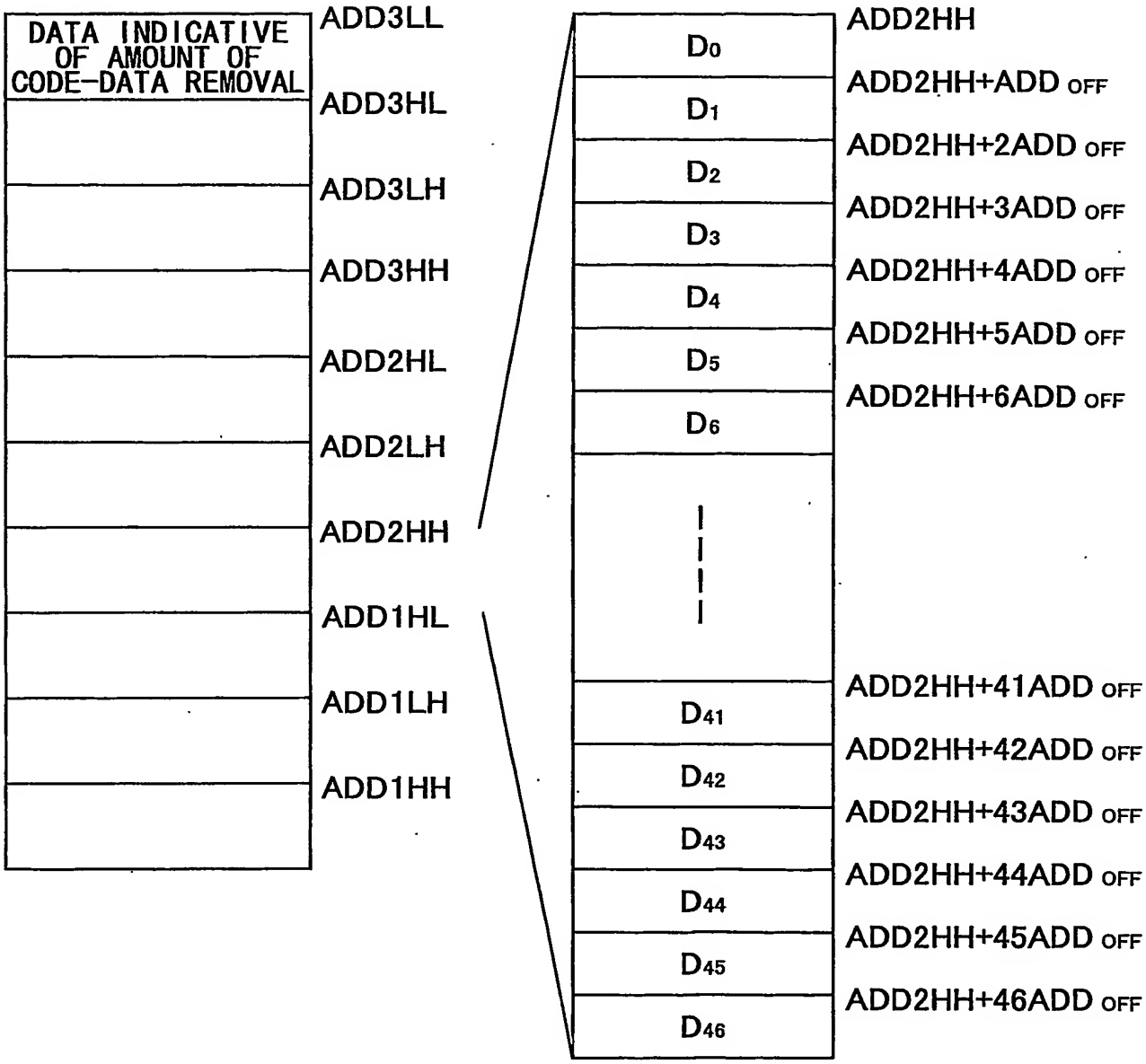

DATA INDICATIVE OF AMOUNT OF CODE-DATA REMOVAL
ADD3LL
ADD3HL
ADD3LH
ADD3HH
ADD2HL
ADD2LH
ADD2HH
ADD1HL
ADD1LH
ADD1HH
D0
D1
D2
D3
D4
D5
D6
D41
D42
D43
D44
D45
D46
ADD2HH
ADD2HH+ADD OFF
ADD2HH+2ADD OFF
ADD2HH+3ADD OFF
ADD2HH+4ADD OFF
ADD2HH+5ADD OFF
ADD2HH+6ADD OFF
ADD2HH+41ADD OFF
ADD2HH+42ADD OFF
ADD2HH+43ADD OFF
ADD2HH+44ADD OFF
ADD2HH+45ADD OFF
ADD2HH+46ADD OFF

FIG.16

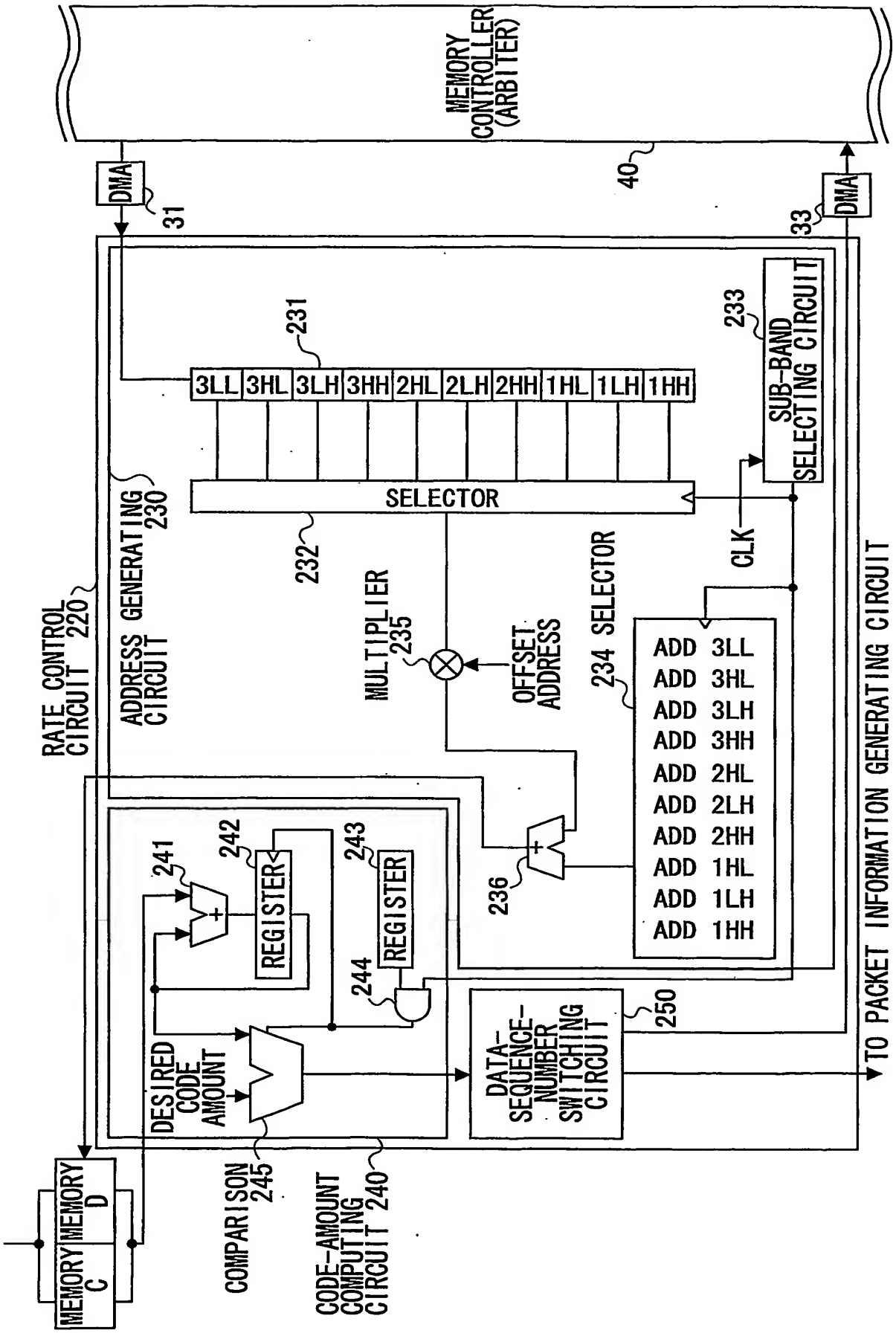

MEMORY CONTROLLER (ARBITER)
40
DMA
31
DMA
33
231
3LL 3HL 3LH 3HH 2HL 2LH 2HH 1HL 1LH 1HH
233
SUB-BAND SELECTING CIRCUIT
SELECTOR
232
ADDRESS GENERATING CIRCUIT 230
RATE CONTROL CIRCUIT 220
MULTIPLIER 235
OFFSET ADDRESS
234 SELECTOR
CLK
ADD 3LL
ADD 3HL
ADD 3LH
ADD 3HH
ADD 2HL
ADD 2LH
ADD 2HH
ADD 1HL
ADD 1LH
ADD 1HH
236
241
242
REGISTER
243
REGISTER
244
DESIRED CODE AMOUNT
DATA-SEQUENCE-NUMBER SWITCHING CIRCUIT
250
TO PACKET INFORMATION GENERATING CIRCUIT
MEMORY C
MEMORY D
COMPARISON 245
CODE-AMOUNT COMPUTING CIRCUIT 240

FIG.17

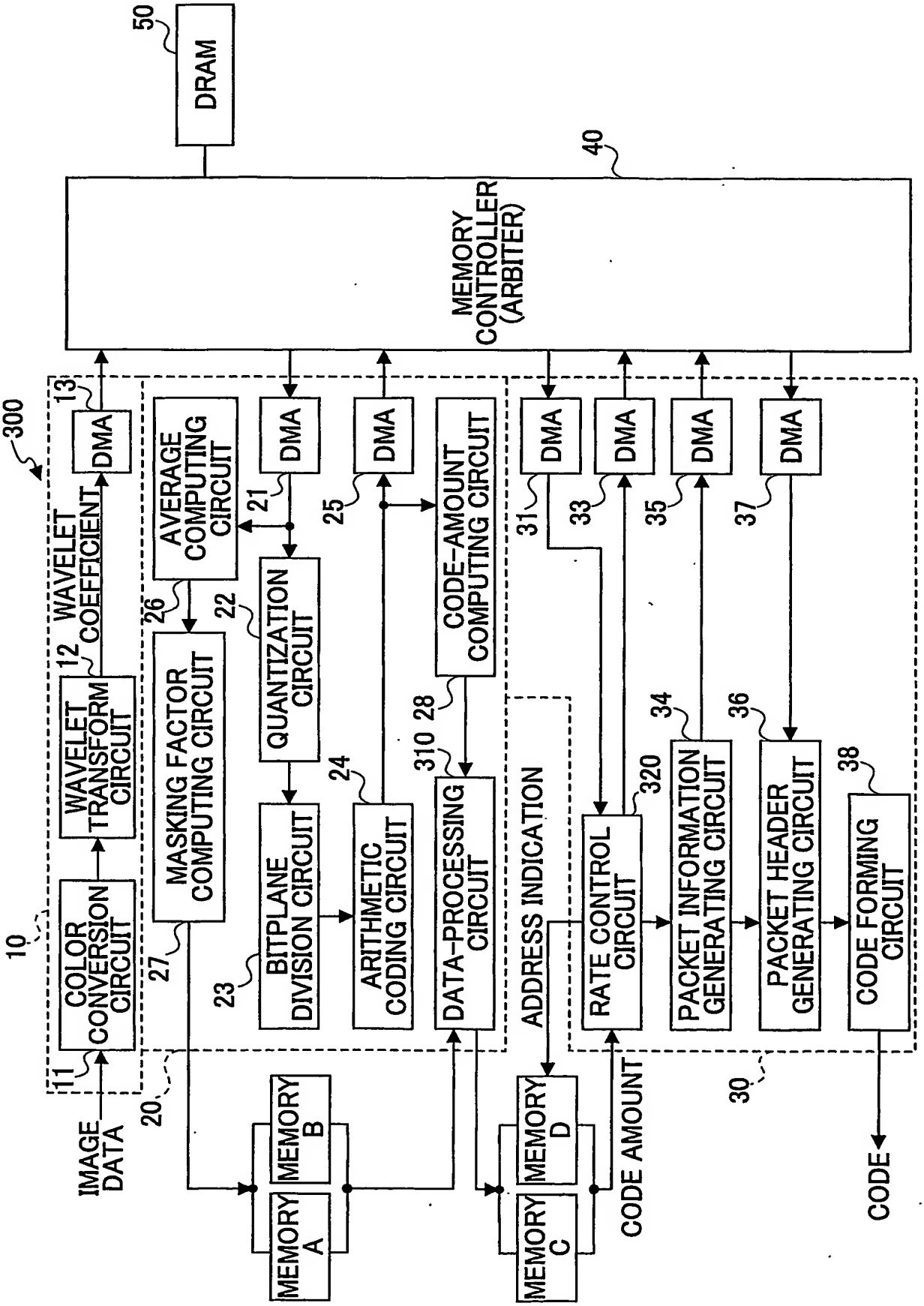

50
DRAM
40
MEMORY CONTROLLER (ARBITER)
300
10
11
COLOR CONVERSION CIRCUIT
IMAGE DATA
12
WAVELET TRANSFORM CIRCUIT
13
DMA
WAVELET COEFFICIENT
20
MASKING FACTOR COMPUTING CIRCUIT
27
AVERAGE COMPUTING CIRCUIT
26
21
DMA
QUANTIZATION CIRCUIT
22
BITPLANE DIVISION CIRCUIT
23
ARITHMETIC CODING CIRCUIT
24
DMA
25
CODE-AMOUNT COMPUTING CIRCUIT
28
DATA-PROCESSING CIRCUIT
310
MEMORY A
MEMORY B
MEMORY C
MEMORY D
ADDRESS INDICATION
CODE AMOUNT
30
DMA
31
DMA
33
RATE CONTROL CIRCUIT
320
DMA
35
PACKET INFORMATION GENERATING CIRCUIT
34
DMA
37
PACKET HEADER GENERATING CIRCUIT
36
CODE FORMING CIRCUIT
38
CODE

FIG.18

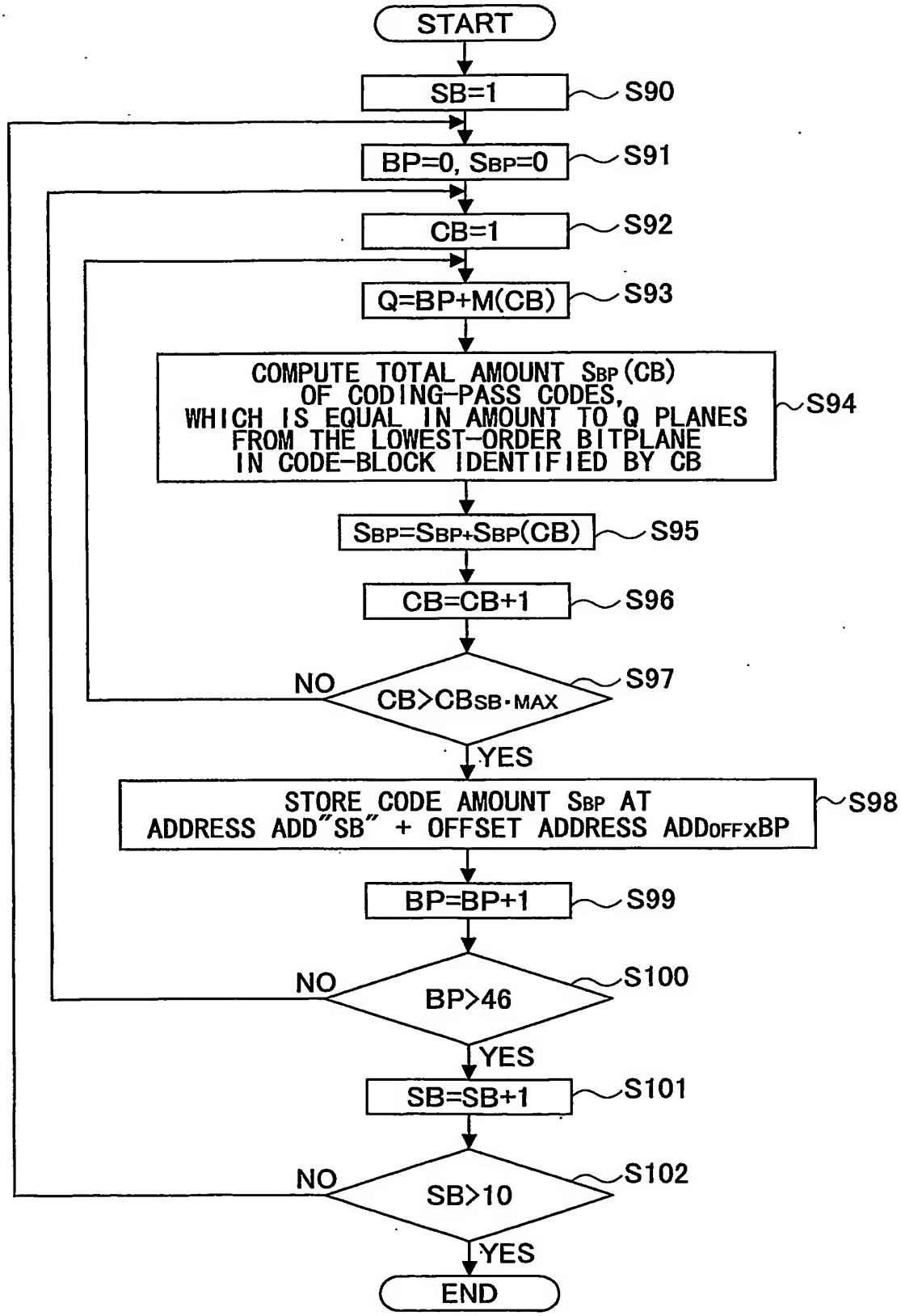
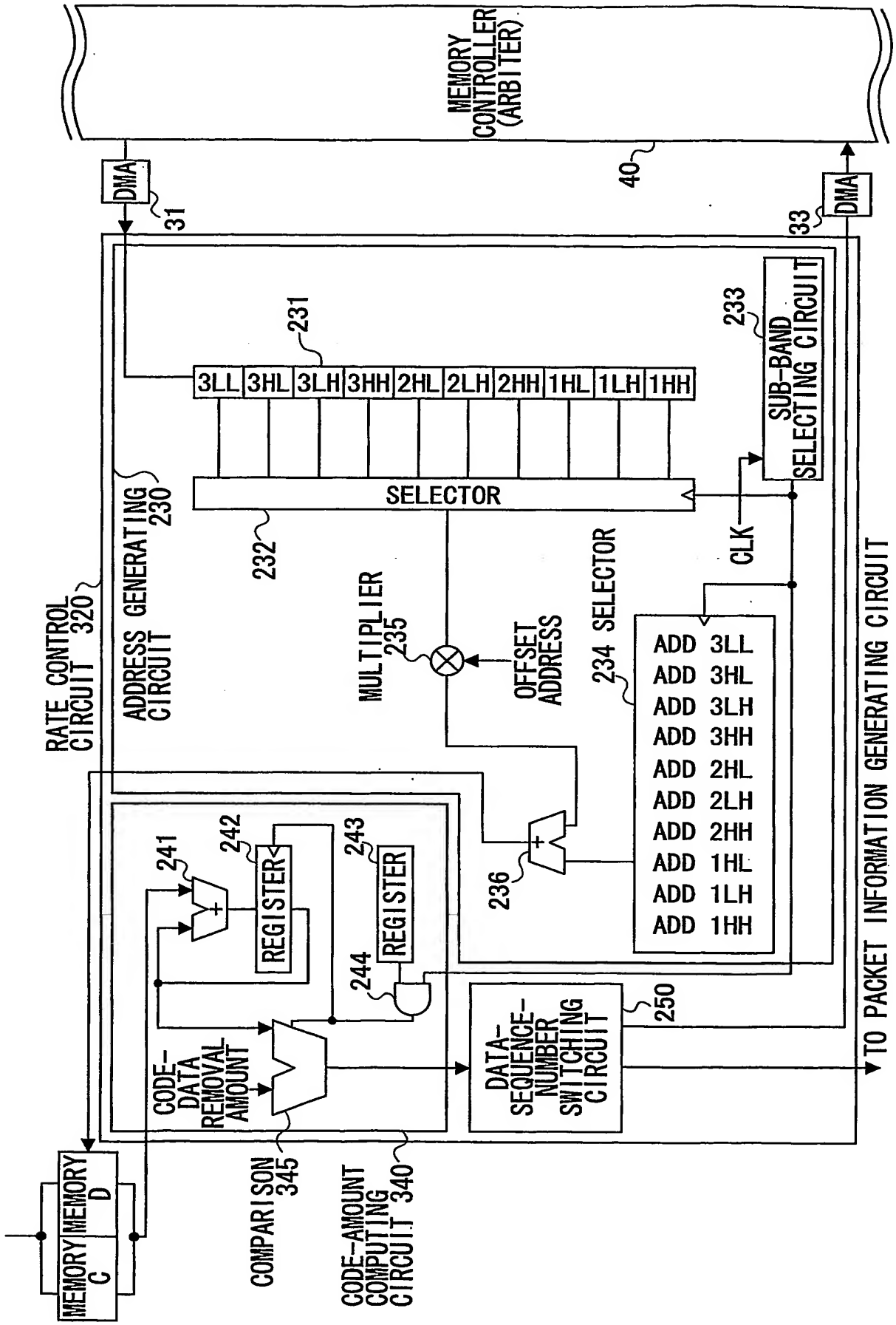

START
SB=1
S90
BP=0, SBP=0
S91
CB=1
S92
Q=BP+M(CB)
S93
COMPUTE TOTAL AMOUNT SBP(CB) OF CODING-PASS CODES, WHICH IS EQUAL IN AMOUNT TO Q PLANES FROM THE LOWEST-ORDER BITPLANE IN CODE-BLOCK IDENTIFIED BY CB
S94
SBP=SBP+SBP(CB)
S95
CB=CB+1
S96
NO
CB>CBSB·MAX
S97
YES
STORE CODE AMOUNT SBP AT ADDRESS ADD"SB" + OFFSET ADDRESS ADDOFFXBP
S98
BP=BP+1
S99
NO
BP>46
S100
YES
SB=SB+1
S101
NO
SB>10
S102
YES
END

FIG.19


MEMORY CONTROLLER (ARBITER)
40
DMA
31
DMA
33
231
3LL 3HL 3LH 3HH 2HL 2LH 2HH 1HL 1LH 1HH
SUB-BAND SELECTING CIRCUIT
233
SELECTOR
232
ADDRESS GENERATING CIRCUIT 230
RATE CONTROL CIRCUIT 320
MULTIPLIER 235
OFFSET ADDRESS
234 SELECTOR
CLK
ADD 3LL
ADD 3HL
ADD 3LH
ADD 3HH
ADD 2HL
ADD 2LH
ADD 2HH
ADD 1HL
ADD 1LH
ADD 1HH
236
241
242
REGISTER
243
REGISTER
244
CODE-DATA REMOVAL AMOUNT
DATA-SEQUENCE-NUMBER SWITCHING CIRCUIT
250
TO PACKET INFORMATION GENERATING CIRCUIT
MEMORY C
MEMORY D
COMPARISON 345
CODE-AMOUNT COMPUTING CIRCUIT 340